Design for Excellence

PCB Layout and Design

Design practices for Printed Circuit Board Assemblies
to achieve design excellence and optimum manufacturability

INTRODUCTION:

In the world of electronics, there are four distinct viewpoints: 1) the inventor, 2) the designer, 3) the manufacturer, 4) the end-user.

One must consider the requirements of all four when striving to develop the most capable product with minimal cost, as all four contribute significantly to the successful outcome of the finished good.

From a contract manufacturer's perspective, variation exists in the design of a printed circuit board (PCB) and the resulting printed circuit board assembly (PCBA). This variation can either 'make or break' the success of consistently building a quality product. Although many guidelines and standards do exist to help define designs that are easier to manufacture, awareness of their existence and the nature of their intent may not be fully or consistently understood.

The purpose of this document is to provide PCBA layout and designers proactive input to the requirements for sound PCBA design and insight to the issues that are commonly found during manufacturing.

Designers who incorporate these design standards and who seek to understand the manufacturing issues prior to the design process tend to deliver more successful designs with fewer design rework cycles ultimately leading to lower overall cost and better performance to schedules.

At the very least, designs should be reviewed with regard to design standards and the following list of concerns and any discrepancies found be resolved prior to having the product built.

INDUSTRY RESOURCES:

IPC (www.IPC.org) is a global trade association serving the printed board and electronics assembly industries, their customers and suppliers. They work to harmonize design and manufacturing standards across the supply chain to achieve optimum quality and cost. The most important standards in PCB layout and design are:

The entire IPC standards tree can be found at:

https://www.ipc.org/4.0_Knowledge/4.1_Standards/SpecTree.pdf

IPC-2581: It is the standard used for sending information between a PCB designer and a manufacturer or assembly company. It helps in delivering a standardized format for exchanging design data that help to ensure consistent production results.

IPC-2221: It is the standard that is used for designing the PCBs, this standard addresses the topics associated with the designing of a PCB such as design, layout, materials, mechanical and physical properties, electrical properties, thermal limitations, parts list and more.

IPC-2141A: Design Guide for High-Speed Controlled Impedance Circuit Boards.

IPC-2152: Standard for Determining Current-carrying Capacity in Printed Board Design.

IPC-7351: Generic Requirements for Surface Mount Design and Land Pattern Standard

Designs intended for fabrication and assembly in IPC compliant shops should comply with these standards in addition to the guidance herein.

CONTRACT DESIGNER RELATIONSHIP:

Communication

Suppliers may not disclose any details of business transactions with Vergent Products to any third party without prior written consent from Vergent Products. Suppliers are expected to notify Vergent Products of any inquiries by a third party concerning our purchase order.

From time to time it may be necessary to engage Vergent Product's client in technical discussions. All verbal and written communications with our clients must include the assigned Vergent Products Program Manager and Process Engineer.

Changes to Purchase Order or Specification

No change shall be made to Vergent Products Purchase Order (PO) or specifications without written approval from the Buyer or a Company Director.

Design Review and Final Acceptance

Prior to the scheduled delivery date and acceptance of the work product, a formal Design Review with interested parties will be scheduled by the Program Manager. The requirements herein will be the basis of this review. A statement of conformity to the design requirements shall be provided at the completion of the project.

PCBA DESIGN TOOL REQUIREMENTS:

Schematics, libraries and PCB layout shall be developed using EDA tools with the following capabilities:

- Schematic
- Net list generation
- PCB Layout
- Universal IPC symbols
- Universal IPC libraries
- Importable into Altium
- ERC
- DRC
- Automated board output file generation

Designs shall use IPC libraries. Exceptions shall be reviewed and approved on a case-by-case basis.

EDA tools are required to have minimal Electrical Rule Checking (ERC) and Design Rule Checking (DRC).

ERC shall be run via the EDA tool**.**

DRC shall be ran after completion of the layout. An automatic program will check all physical connections in the design against standard design rules and report any violations.

Where possible the PCB fab DRC shall also be ran to identify any errors or warnings.

The goal is to zero errors and zero warnings in ERC, DRC, and fab DRC checks.

VERGENT PRODUCT DESIGN STANDARDS:

The following design standards are expected to be implemented on designs for Vergent Products. It is understood that some of these requirements may be impossible for certain designs. Omission should by exception with mutual agreement during the design process.

Design inputs:

Design input should incorporate the following (minimum input) provided by Vergent Products:

1. Expected production quantities.
2. Solder Technology (No clean, Tin/Lead, RoHS, etc)
3. IPC Class
4. Number of SMT sides preferred
5. Number of PTH sides preferred
6. Open or closed AML
7. Broker parts acceptable
8. Registered pricing
9. Inventory optimization (cost or excess inventory)
10. FOD control requirements
11. Coating requirements
12. Panelization preferences
13. Impedance controlled
14. Copper weight
15. Maximum differential voltage
16. Method of programming firmware (JTAG, connector, pads)
17. Method of test (if ICT or bed of nails, refer to Test appendix)
18. Regulatory requirements (UL, CE, CSA, FDA, FCC, etc)
19. Schematic diagram
20. Bill of Materials
21. Part Number of the product
22. Copyright year and ownership
23. Export control status

Design outputs (electronic data):

The following data is required:

1. Gerber data (layers, silkscreen, masking, paste layers, drills)
2. Component placement data (Centroid with X/Y/theta information)
3. Schematics are required for test development and troubleshooting.
4. PCB Fabrication drawing (fab notes, dimensions, raw board test requirement)
5. If impedance controlled a layer stack up illustration
6. Assembly drawings (back add details, adhesives, potting, heatsinks, daughters, etc)
7. Conformal coating drawings (show masking, call out materials and thickness)
8. Bill of Materials (BOM) with reference designators in Microsoft Excel or ASCII format
9. Regulatory requirements.

Fabrication notes:

Fabrication notes for PCBs must be included with Gerber data or in an appropriate assembly or fabrication document. Fabrication notes should include:

- IPC class for the fabrication of the PCB per IPC-6012 current rev.
- IPC class for the acceptability of the PCB per IPC-A-600 current rev.
- IPC class for finished assembly of the PCBA IPC-A-610 current rev.
- A RoHS statement if the PCBA must be RoHS complaint.
- A statement or laminate stack up drawing specifying the Tg. (ie: Tg > 170C)
- A statement or drawing specifying the finish (ie: Electroless Nickel Immersion Gold (ENIG)).
- A statement specifying the color of solder mask (ie: Green).
- A statement specifying the color of silkscreen (ie: White).
- A statement or laminate stack up drawing specifying the number of layers, copper weight, board thickness. (ie: PCB is six layers, 1oz. outer copper layers, 0.5oz. inner copper layers, .063" ±10% thick).
- A statement specifying trace & space minimums (ie: trace/space = .008" minimum).
- A statement specifying smallest hole size (ie: smallest hole = .018" diameter).
- Drill chart
- A statement specifying greatest potential difference on the PCBA. (ie: Max V = 50 V).
- A statement specifying cleanliness requirement (ie: No-clean flux residue visible at 4X magnification).
- A list of parts that cannot be washed: (ie: Transducer @ PSS1, SW1, SW2, K1 cannot be washed)

Copyrights/Export Control:

The following statements should appear on all documentation:

- Vergent Products 609 14th Street SW, Loveland, CO, 80537
- Vergent Products Confidential
- Copyright {year} {Client Name}
- Current Revision
- Revision Block
- Document Author
- Part Number
- Date Released

If the product is export controlled the following statement must appear on all documents:

"WARNING This document contains technical data whose export is restricted by the Arms Export Control Act (Title 22, U.S.C., Sec 2751, et seq.) or the Export Administration Act of 1979 (Title 50, U.S.C., App. 2401 et seq.), as amended. Violations of these export laws are subject to severe criminal penalties. Disseminate in accordance with provisions of DoD Directive 5230.25."

If the product is export controlled all documentation must be encrypted "at-rest" and "in-transit". Refer to Vergent Products CWP-021 Export Management and Compliance Program

Fiducials are required.

Each panel should contain at least three fiducials, two of which are diagonal and as far apart from each other as possible. The third should be in the same plane as at least one of the other two fiducials. Each fiducial should be finished copper measuring .040" in diameter with a .100" keep-out area that is relieved of copper and free of any silkscreen, attribute, or other material that would jeopardize the contrast required for successful automated registration. In simple terms, think about a donut and maybe even draw one. The donut hole represents the .040" finished metal fiducial, the actual donut is the keep out area and the outer circle would represent the outside perimeter of that keep-out area. Fiducials need to be inboard of the panel edge by at least .200" to ensure they are not covered by any clamping mechanisms inherent to the automated manufacturing equipment. Additional panel material will be required if these fiducials are too close to the edge. Furthermore, it is recommended that each PCB within an arrayed panel employ this three-fiducial format.

Polarity marks exist and are visible after component is installed:

All polarized locations should have corresponding polarity marks that are either silkscreened onto the PCB or are included in the copper layer. Having these polarity marks visible after the component is installed is essential for prompt and accurate post-install verification.

Clear diode orientation:

Diodes require a polarity mark. Symbols such as '+' or '-' tend to be ambiguous when working with diodes and should be avoided. Use the schematic diode symbol is widely accepted and symbols 'C' or a 'K' on the cathode side and an 'A' on the anode side work as well.

Appropriate Lead/Hole-size relationship:

Adequate space in the lead-to-hole-size relationship of through-hole applications is very important and must be accounted for when the PCB is designed. This can directly affect vertical fill of solder and top-side wetting on through-hole designs by improving capillary action. It can also directly affect the success of automated insertion. The finished hole-size should be at least .019" larger than the diameter of the lead that accompanies it. Universal Instruments® also recommends a .019" delta when through-hole components are inserted with high-speed insertion equipment. In this model, the diameter across a square lead would be the distance across opposite corners (hypotenuse.)

Tabs/mousebites:

Tabs are used to connect PCBs within a routed panel. Mousebites are the perforations or holes that accompany these tabs to allow the cleanest results upon separation. General specifications for a .063" thick PCB with average component density might be .050" wide tabs placed approximately every 2" with mousebites that consist of .018" holes placed on the center of the PCB edge at .028" pitch. Larger, thicker and heavier designs will certainly benefit from wider tabs. Remember to relieve internal copper from the PCB edge and distance any nearby traces from these tab/mousebite locations to prevent exposed copper or damaged traces upon separation. It is best to consult with process engineers if in doubt.

Panel breakaways interference with overhanging components or features:

Panel design should allow adequate relief for anything that might overhang the edge of the PCB, such as a connector or other feature. Tabs/mousebites should not be placed under any physical attribute that may interfere with the de-paneling process. Fortify the PCB Gerber data with relief information, as well as any 'keep-out' areas that would clearly define locations that a tab/mousebite cannot go, such as under an overhanging connector or near a trace that simply cannot be moved inward from the PCB edge. This information is also helpful when scoring is used.

Components too close to edge:

Manufacturing equipment clamping mechanisms require un-obstructed room to grab the PCB effectively. Will the PCB require extra panel material that is removed once manufacturing is complete? Delicate components, such as MLCC, are at risk of cracking when they are placed too close to the edge. MLCC must be at least .3" from board edge.

Dry parts:

Devices such as tactile switches, buzzers, speakers, batteries, and loosely wound inductors are but a few that may not be wash-friendly. Washing these devices may cause damage or they might be difficult to dry, thus requiring them to be installed using more expensive manual methods after the wash process is complete. Consider sealed alternatives that can survive the wash. Clearly communicate any components that cannot be washed. No-clean processes do not require wash but leave flux residue that some clients may not want.

Vias in pads:

No vias in pads are allowed.

Un-masked vias:

Design with at least .015" or more of solder mask to serve as a solder dam that separates the pad from the un-masked via.

Un-masked vias/solder dams under BGA devices:

Mask the vias directly under BGA devices except on thermal pads.

Solder mask at fine pitch locations:

Fine pitch devices are defined as those having a lead pitch, or the distance between the centers of two adjacent leads, of less than or equal to .025" (.635mm). Solder mask between the pads of fine pitch devices is required to reduce the chance of bridging defects. The mask must be at least a .004" wide for adequate adhesion to the PCB laminate.

Different pad sizes for BGAs:

BGA pads must be uniform size.

Mixed SMD and NSMD approaches to BGAs:

Solder Mask Defined and Non Solder Mask Defined applications should not be shared under the same device. NSMD is preferred over SMD for the sake of reliability per IPC-7095.

Lead-free solder balls on BGAs in a leaded design:

Different solder alloys often require different thermal profiles for successful reflow. Always communicate when lead-free BGAs are used in a design that requires leaded solder.

Large deltas in thermal mass across assembly:

Large deltas in thermal mass, across components and internal to the PCB itself, can make it more challenging if not impossible to reach thermal equilibrium before the liquidus solder event occurs. Keep in mind that different thermal masses reach preferred temperatures at different rates. This can lead to tombstones, laminate bow and twist, failure to collapse on BGA devices, inconsistent solder quality, etc.

Thermal relief:

Vertical fill and top-side wetting in a wave solder process is dependent on heat. Thermal relief improves the ability to reach the temperatures required to achieve quality solder joints on through-hole devices and can also be very useful to balance surface mount land patterns associated with smaller packages. Its importance increases as thermal mass increases - the result of heavier ground planes and components, more layers and designs that use two ounce or greater copper. Ensure that adequate thermal relief exists throughout the design.

Traces that promote natural bridging:

No features with short inter-pad traces. These features promote natural bridging which create confusion and error during inspection when bridges appear to be a defect. As such, the assembler will attempt to remove the defect often damaging the board. Inspectors become de-sensitized to these anomalies and miss real bridges.

Oversized geometry on thermal lugs:

Devices with large center areas requiring solder are prone to bridging especially if the perimeter connections are very close to the center lug. A custom aperture design may be required here to reduce the amount of solder paste if you are designing the SMT solder paste layer.

Packages fit:

Consult IPC-7351 and datasheets for proper land design and package fit. Poorly spaced pads can lead to defects such as tombstone, drawbridge, no component and poor heel fillets.

Courtyard issues – repair ability:

At least .150” of open space around BGAs or any other devices that require hot air for rework.

Close proximity of high profile components such as electrolytic capacitors, tall relays, or connectors can make it impossible to achieve adequate reflow temperatures for those devices without over-exposing the rest of the assembly. Spread things out or revise the layout to support the ability to solder the entire assembly. Design with the ability to rework in mind.

Solder and flux requirement:

Some designs require special solders and fluxes. Be sure to communicate these special requirements.

RoHS component thermal considerations

Components selected for RoHS assemblies must be able to survive the lead-free solder processing at 260°C.

PCB finish:

Electroless Nickel Immersion Gold (ENIG) finish is required for assemblies containing fine pitch, any bottom terminated component, or 0402 or smaller components. Immersion Silver (ImAg) is an acceptable substitute but shelf life is 3 months.

Lead-free RoHS-compliant Hot Air solder Level (HASL) is acceptable.

Lead Hot Air solder Level (HASL) is acceptable when RoHS is not a required.

Organic Solder Preservative (OSP) and Immersion Tin (ImSn) are not supported finishes

Definition of laminate stack:

PCB's vary in the number of layers, copper weight and overall thickness. These variables must be defined in the fabrication notes and drawing.

Impedance controlled boards require a laminate stack-up drawing.

IPC classification declaration:

IPC standards are used by Vergent Products and our supply chain. Workmanship specifications must be clearly identified in fabrication notes and assembly drawings.

IPC-A-600 covers the raw PCB.
IPC-A-610 regards the finished PCBA.

The quality tiers are:

Class 1 – General Electronics Products, basically the device has to function. Examples of devices in this category are toys, disposable electronics, novelties.

Class 2 – Dedicated Service Electronic Products, products where continued performance and extended life is required but uninterrupted service is not critical. Most durable consumer and industrial designs fit this category.

Class 3 – High Performance Electronics Products, high performance products where continued or on-demand functionality is critical. Avionics, Medical, Life Safety, Defense products fit this category.

Maximum potential voltage identified:

IPC specifies minimal electrical clearance that are determined by the amount of voltage inherent to a specific product. The greatest potential voltage differential must be clearly specified in fabrication notes and assembly drawings.

PCB base-material laminate specification:

IPC-4101 standard identifies these laminate specifications. The laminate must be specified in fabrication notes. RoHS designs require a minimum glass transition temperature or Tg ≥ 170°C.

Label location:

A location for a 1.0” x .25” label is recommended for assemblies requiring serialization. Smaller labels are possible – consult with process engineering if a different label sized is required.

Gerber legend required:

Include a legend that decodes Gerber layer filenames and extensions. This legend is best located in the Gerber data but may also reside in a README.TXT file that accompanies the data.

Regulatory Requirements:

Clearly identify all regulatory requirements in fabrication notes and assembly drawings.

Multi source AVL/AML:

Where possible provide least two sources for each component whenever Approved Vendor List (AVL) and Approved Manufacturer List (AML) source control is required.

Regulated components:

Identify any component governed by a regulatory agency, such as UL, ETL, CE, or others.

Torque specification:

Torque specifications are required for any fasteners on the assembly drawing.

Design Checklist

DfX consideration	Check
Inputs complete?	
Outputs complete?	
Fabrication notes compliant?	
Titles, Copyrights, and Export Control statements?	
Fiducials inadequate or missing?	
Polarity marks exist and are visible after component is installed?	
Is diode orientation identified clearly?	
Minimal Lead/Hole-size relationship?	
Tabs/mousebites?	
Panel breakaways interference?	
Components too close to edge?	
Dry parts exist?	
Are there vias in pads?	
Are un-masked vias far enough away from the solder site?	
Un-masked vias or inadequate solder dams under BGA devices?	
Solder mask at fine pitch locations?	
Different pad sizes for BGAs?	
Mixed SMD and NSMD approaches to BGAs?	
Lead-free solder balls on BGAs in a leaded design?	
Large deltas in thermal mass across assembly?	
Thermal relief?	
Traces that promote natural bridging?	
Oversized geometry on thermal lugs?	
Do wire modifications exist?	
Do packages fit the pads?	
Really small components, really fine pitch, leadless devices?	
Courtyard issues, are devices too close?	
Devices that are difficult or cannot be reworked post assembly?	
Is no-clean flux residue acceptable?	
Are trace cuts required?	
SMT verses PTH mix?	
Is the product controlled by RoHS?	
RoHS temperature complent?	
Is the PCB finish clearly identified?	
Is the laminate stack clearly defined?	
Is ‘trace & space’ and smallest hole diameter identified?	
Are build standards identified?	
Maximum potential voltage identified?	
PCB base-material laminate specs missing or inadequate?	
Does a location exist for a label?	
Does a legend exist for Gerber layer files?	
Does the product have Regulatory Requirements?	
Multi source AVL/AML?	
Torque specifications identified?	

APPENDIX – Design for Test

These guidelines are applicable to ICT. Tooling holes and test points are applicable to any assembly being tested on bed of nails fixtures.

TOOLING HOLES:

Tooling holes (non-plated through) should be located on the board at diagonally opposing corners

- Tolerance from DUT Datum to test pads should be +/-.002"
- Tolerance between tooling holes should be +1-.002"
- Tooling hole diameter should be .125" with a tolerance of +.003"/-.000"
- Tooling holes should have a .125" annulus of free space from components and edges

TEST POINTS:

If possible provide probe access to every net on the board.

All test points should be accessible from the bottom side of the board

- Test point pad diameters should be a minimum of .035"/.040"
- Minimum spacing between test point pad edges should be .015"
- Test pads should be .100" center spacing if possible
- Minimum distance between any test point and the edge of the board should be .100"/.250"
- Test pad or test via should have a .018" annulus of free space from components
- Test pad or test via must be solder coated
- Distribute test point pads/vias evenly and ensure they are accessible after assembly.
- Provide alternate test point pads or test point vias when possible

COMPONENTS AND CIRCUITS:

Components on bottom side of board should be limited to .250" in height, and should not obstruct any test points or test vias.

- Place test pads or test vias .200" away from components taller than .250"
- Component pads or component leads should not be considered a test point
- Components with no-connects should include test points routed to the bottom side
- Top side component traces should include test points routed to the bottom side
- All electrical signals must have an associated test point pad or test point via

All components should be a minimum of 0.125 inch from the board edge or tooling holes. Exceptions to this are components that require interfacing off the edge of the PCB (i.e. LEDs, connectors, switches).

Resistors with a value between 470 ohms and 2.2K ohms generally found on the BOM, should be designed into the disable circuitry of all logic devices to provide ICT with a means of disabling those devices

Jumpers, 0 ohm resistors, fuses, SPST switches are considered two lead components, therefore each node requires a separate test point pad or test point via.

Provide a means to disable every IC on the board either through Boundary Scan, one pin disables, or acc ess to an output enable pin that is not hard tied to power or ground.

Use individual pull-up or pull-down resistors on enable pins so devices can be disabled independently.

Use resistors to connect inputs to power or ground.

Provide probe access to every net on board.

A minimum of one ground probe point for every 32 nodes on the board.

One power probe point for every .2 amps of current the board draws on any particular power input.

Provide access to all Boundary Scan TAP pins (TDI,TDO,TMS,TCK,TRST) and do not hard connect any of these pins to power or ground.

All oscillators should be tri-stateable, gated, or strapped to allow tester control from a test point.

Provide a means to disable clock circuits and allow for insertion of a “test” clock.

BGAs:

Guidelines for testing BGA devices are as follows:

- Must have 100% access to all pins of the BGA from the bottom side of the PCBA including all 'no connects'. Pads should be no less than .025" diameters. (.018" for micro BGAs)
- Must have 100% access from the bottom side for the JTAG (or TAP) for each BGA
- The JTAG (or TAP) should be IEEE 1149.1 - 1990 and IEEE 1149.1- 1993 compliant.
- Will need the BSDL from the manufacturer of the BGA for creating a digital test
- If the thickness of the PCB is less than .062" do not locate the test points (vias) directly underneath the BGA, spread them out so as to reduce the stress directly to the BGA's connections.
- If you must put test points (vias) directly underneath the BGA, place no more than 30 test points per 1 square inch of space equally separated.
- Must have at least .200"in spacing around the BGA on the top side. This is to put a special pressure frame to keep the PCBA from flexing under test.

DOCUMENTS AND MATERIALS:

The following documentation and materials should be provided at the start of ICT development:

- Schematic (.pdf, .dfx, .sch as well as any other Electronic format)
- Parts List (BOM and NET in ASCII format)
- Assembly and fabrication drawings
- Drill files in ASCII format (test point XY)
- CAD Data in ASCII format (including netlist, component data, and geometry-x/y data) preferably MENTOR CAD format or GENCAD or any other CAD.
- JEDEC files for programmable devices. These files should be provided, otherwise, test vectors cannot be generated and those devices will be considered untestable.
- Current revision raw PCB and populated